

B
a first silicon nitride layer provided by a CVD method on said silicon oxide layer; and

a second silicon nitride layer provided on said first silicon nitride layer and having a lower trap density than that of said first silicon nitride layer.

Rewrite claim 5 as follows:

C2
B
5. A non-volatile semiconductor memory device comprising:
a semiconductor substrate; and
a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,
wherein silicon nitride layers formed by a CVD method have a given trap density and said inter-insulating layer includes:
a silicon oxide layer contiguous to said floating gate; and
a silicon nitride layer deposited on said silicon oxide layer and having a lower trap density than that of said given trap density.

Rewrite claim 7 as follows:

C2
B3
7. A non-volatile semiconductor memory device comprising:
a semiconductor substrate; and
a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,



wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon nitride layer deposited on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/\text{cm}^3$ or less.

Rewrite claim 9 as follows:

- C2
9. A non-volatile semiconductor memory device comprising:
- a semiconductor substrate; and
- a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,
- wherein silicon nitride layers formed by a CVD method have a given trap density and said inter-insulating layer includes:
- a silicon nitride layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a lower trap density than that of said given trap density.
- 14

Rewrite claim 11 as follows:

11. A non-volatile semiconductor memory device according to claim 9, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and
- 13

still further including a silicon oxide layer interposed between said double-layered silicon nitride layers.

13 [Rewrite claim 12 as follows:]

12. A non-volatile semiconductor memory device according to claim 9, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and

still further including a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method interposed between said double-layered silicon nitride layers.

Rewrite claim 14 as follow:

14. A non-volatile semiconductor memory device comprising:
a semiconductor substrate; and
a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,
wherein said inter-insulating layer includes:
a silicon nitride layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a quantity of hydrogen content on the order of $10^{19}/\text{cm}^3$ or less.

Rewrite claim 16 as follows:

13X
16. A non-volatile semiconductor memory device according to claim 14, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and still further including a silicon oxide layer interposed between said double-layered silicon nitride layers.

[Rewrite claim 17 as follows:]

17. A non-volatile semiconductor memory device according to claim 14, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and still further including a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method interposed between said double-layered silicon nitride layers.
